CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming an electrode comprising:

forming a dielectric layer over a first conductive layer;

forming an opening in said dielectric layer so as to expose a portion of said first conductive layer;

forming an adhesion layer over said dielectric layer and said exposed portion of said first conductive layer;

forming a second conductive layer over said adhesion layer; and

forming a third conductive layer over said second conductive layer and said adhesion layer within said opening.

2. The method of claim 1, wherein said step of forming a second conductive layer further comprises planarizing said second conductive layer and said adhesion layer such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

3. The method of claim 2, further comprising the step of recessing said second conductive layer and said adhesion layer within said opening.

4. The method of claim 3, wherein said step of forming a third conductive layer further comprises planarizing said third conductive layer such that a top surface of

said third conductive layer is substantially level with a top surface of said dielectric layer.

5. The method of claim 1, wherein said adhesion layer is formed from on one of an oxide and a nitride.

6. The method of claim 5, wherein said adhesion layer is titanium nitride.

7. The method of claim 1, wherein said first conductive layer is formed from at least one of the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

8. The method of claim 1, wherein said second conductive layer is tungsten.

9. The method of claim 1, wherein said third conductive layer is formed from a same material as the first conductive layer.

10. The method of claim 1, wherein said third conductive layer is formed from a same material as the second conductive layer.

11. A method of forming an electrode comprising:

forming a dielectric layer over a first conductive layer;

forming an opening in said dielectric layer so as to expose a portion of said first conductive layer;

forming an adhesion layer over said dielectric layer and said exposed portion of said first conductive layer;

forming a second conductive layer over said adhesion layer;

forming a third conductive layer over said second conductive layer and said adhesion layer within said opening; and

patterning said third conductive layer.

12. The method of claim 11, wherein said step of forming a second conductive layer further comprises planarizing said second conductive layer and said adhesion layer such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

13. The method of claim 12, further comprising the step of recessing said second conductive layer and said adhesion layer within said opening.

14. The method of claim 11, wherein said third conductive layer is patterned using photolithography and dry etching.

15. The method of claim 11, wherein said adhesion layer is formed from one of an oxide and a nitride.

16. The method of claim 11, wherein said adhesion layer is titanium nitride.

17. The method of claim 11, wherein said first conductive layer is formed from at least one of the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

18. The method of claim 11, wherein said second conductive layer is formed from tungsten.

19. The method of claim 11, wherein said third conductive layer is formed from the same material as the first conductive layer.

20. The method of claim 11, wherein said third conductive layer is formed from the same material as the second conductive layer.

21. An electrode having minimal workfunction variation, comprising:

a first conductive layer;

a dielectric layer over said first conductive layer, said dielectric having an opening exposing a portion of said first conductive layer;

an adhesion layer over said dielectric layer and said exposed portion of said first conductive layer;

a second conductive layer over said adhesion layer, wherein said second conductive layer and said adhesion layer are recessed within said opening in said dielectric layer; and

a third conductive layer over said dielectric layer and over said second conductive layer and said adhesion layer within said opening.

22. The electrode of claim 21, wherein said third conductive layer is planarized such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

23. The electrode of claim 21, wherein said third conductive layer is patterned.

24. The electrode of claim 21, wherein said adhesion layer comprises an oxide or a nitride.

25. The electrode of claim 21, wherein said adhesion layer comprises titanium nitride.

26. The electrode of claim 21, wherein said first conductive layer comprises at least one of the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

27. The electrode of claim 21, wherein said second conductive layer comprises tungsten.

28. The electrode of claim 21, wherein said third conductive layer is formed from a same material as the first conductive material.

29. The electrode of claim 21, wherein said third conductive layer is formed from a same material as the second conductive material.

30. A resistance variable memory device, comprising:

a variable resistance memory element formed over an electrode structure, said electrode structure comprising:

a first conductive layer;

a dielectric layer over said first conductive layer, wherein an opening in said dielectric exposes a portion of said first conductive layer;

an adhesion layer over said dielectric layer and said exposed portion of said first conductive layer;

a second conductive layer over said adhesion layer, wherein said second conductive layer and said adhesion layer are recessed within said opening;

a third conductive layer over said dielectric layer and over said second conductive layer and said adhesion layer within said opening; and

a fourth conductive layer formed over said variable resistance memory element.

31. The resistance variable memory device of claim 30, wherein said variable resistance memory element is a chalcogenide glass having metal ions dissolved therein.

32. The resistance variable memory device of claim 30, wherein said variable resistance memory element is a molecular memory element.

33. The method of claim 30, wherein said third conductive layer is planarized such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

34. The resistance variable memory device claim 30, wherein said third conductive layer is patterned.

35. The resistance variable memory device of claim 30, wherein said adhesion layer comprises one of an oxide and a nitride.

36. The resistance variable memory device of claim 30, wherein said adhesion layer comprises titanium nitride.

37. The resistance variable memory device of claim 30, wherein said first conductive layer comprises at least one of the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

38. The resistance variable memory device of claim 30 wherein said second conductive layer comprises tungsten.

39. The resistance variable memory device of claim 30, wherein said third conductive layer comprises a same material as the first conductive layer.

40. The resistance variable memory device of claim 30, wherein said third conductive layer comprises a same material as the second conductive layer.

41. A memory system, comprising:

an array of memory devices, each memory device having an electrode structure comprising:

a first conductive layer;

a dielectric layer over said first conductive layer, wherein an opening in said dielectric exposes a portion of said first conductive layer;

an adhesion layer over said dielectric layer and said exposed portion of said first conductive layer;

a second conductive layer over said adhesion layer, wherein said second conductive layer and said adhesion layer are recessed within said opening;

a third conductive layer over said dielectric layer, said second conductive layer and said adhesion layer within said opening; and

a fourth conductive layer formed over said variable resistance memory element.

42. The memory system of claim 41, further comprising a variable resistance memory element.

43. The memory system of claim 42, wherein said variable resistance memory element is a chalcogenide glass having metal ions dissolved therein.

44. The memory system of claim 42, wherein said variable resistance memory element is a molecular memory element.

45. The memory system of claim 41, wherein said third conductive layer is planarized such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

46. The memory system of claim 41, wherein said third conductive layer is patterned.

47. The memory system of claim 41, wherein said adhesion layer comprises one of an oxide and a nitride.

48. The memory system of claim 41, wherein said adhesion layer comprises titanium nitride.

49. The memory system of claim 41, wherein said first conductive layer is formed from at least one of the group consisting of tungsten, nickel, tantalum, aluminum, platinum, and conductive nitrides.

50. The memory system of claim 43, wherein said second conductive layer comprises tungsten.

51. The memory system of claim 43, wherein said third conductive layer comprises a same material as the first conductive layer.

52. The memory system of claim 43, wherein said third conductive layer comprises a same material as the second conductive layer.

53. A processor system, comprising:

a processor; and

a memory circuit electrically coupled to said processor, said memory circuit having an electrode structure comprising:

a first conductive layer;

a dielectric layer over said first conductive layer, wherein an opening in said dielectric exposes a portion of said first conductive layer;

an adhesion layer over said dielectric layer and said exposed portion of said first conductive layer;

a second conductive layer over said adhesion layer, wherein said second conductive layer and said adhesion layer are recessed within said opening;

a third conductive layer over said dielectric layer, said second conductive layer and said adhesion layer within said opening.

54. The electrode of claim 53, wherein said third conductive layer is planarized such that a top surface of said layers is substantially level with a top surface of said dielectric layer.

55. The electrode of claim 53, wherein said third conductive layer is patterned.

56. The electrode of claim 53, wherein said adhesion layer comprises an oxide or a nitride.

57. The electrode of claim 53, wherein said adhesion layer comprises titanium nitride.

58. The electrode of claim 53, wherein said third conductive layer is formed from a same material as the first conductive material.

59. The electrode of claim 53, wherein said third conductive layer is formed from a same material as the second conductive material.